Biographies

Adamovich, Vadim I. [3C.4]
Vadim I. Adamovich joined UDC in 2002, as a Senior Scientist. He received his B.S. and M.S. in chemical and nuclear engineering from Mendeleev Univ. of Chemical Technology, Moscow, Russia, and Ph.D. in chemistry from the Univ. of Southern CA in 2002 under the advisement of Professor Mark E. Thompson. Dr Adamovich has over 20 publications and over 10 patents and pending patents in the field of organic light emitting devices (OLEDs). At UDC, he is working on improvement the performance of Phosphorescent OLEDs on the device level.

Agostinelli, Marty [TR06]
Marty Agostinelli received his B.S.E.E. from Louisiana State Univ. (1988), and an M.S.E.E. (1990) and Ph.D. (1993) from the UT Austin. In 1996, he received an M.S. in computer science from the Oregon Graduate Institute. He joined Intel Corp. in 1993 and has been involved in device modeling as well as transistor reliability for Intel's advanced process technologies. Currently, he is responsible for device reliability for advanced process technology development.

Ahmed, Khaled [1.1]
Khaled Ahmed received B.S. (1991) and M.S. (1994) from Ain Shams Univ., Cairo, and the Ph.D. (1998) from NC State Univ., Raleigh, all in electrical engineering. In 1997, he joined AMD, Sunnyvale, CA as intern where he worked on advanced gate dielectrics for high-performance CMOS applications. In 1998, he joined AMD as a Senior Engineer where he worked on MOS device characterization and reliability for logic and nonvolatile memory applications. In 1999, he joined Conexant Systems, Newport Beach, CA where he worked on advanced gate dielectrics for CMOS applications. In 2001, he joined the Front End Products Group, Applied Materials, Sunnyvale, where he is Senior Member of Technical Staff and has been working on the electrical characterization and reliability of ultrathin oxynitrides and high-k gate dielectrics for CMOS applications. He has authored or coauthored over 30 publications. Dr. Ahmed has served as a Technical Program Committee Member for the IRPS (IRPS) and the IEEE Semiconductor Interface Specialists Conference (SISC).

Ahn, Hyun [4D.2]
Hyun Ahn received the B.S. (1990), M.S. (1993) and Ph.D. (2000) in nuclear engineering from Seoul National Univ., Seoul, Korea. Since 2000, he has been a Member of Technical Staff at the Memory R&D division, Hynix Semiconductor Inc., Kyoungki-Do, Korea. His research interests include plasma processing using thermal/cold plasma, plasma diagnostics (OES, SEERS), plasma apparatus for etching, plasma damage in the device integration.

Aikawa, Hisanori [MY01]
Hisanori Aikawa received the B.S. (1999) and the M.S. (2001) in physics from Osaka Univ., Osaka, Japan. In 2001, he joined Toshiba Corp as a scientist in the Corporate Research & Development Center and worked on the HDD media development. Since 2002, he has been worked on MRAM. He is involved in MRAM integration technology, device simulations, and device characterizations in the Corporate Research & Development Center.

Alam, Muhammad Ashraful [1.1; 1.2]
Muhammad Ashraful Alam is a Professor of Electrical and Computer Engineering at Purdue Univ. where his research and teaching focus on physics, simulation, characterization and technology of classical and novel semiconductor devices including theory of oxide reliability, nanocomposite thin film transistors and nano-bio sensors. From 1995 to 2001, he was with Bell Labs, Lucent Technologies, Murray Hill, NJ, as a Member of Technical Staff in the Silicon ULSI Research Dept.. From 2001 to 2003, he was a Distinguished Member of Technical Staff at Agere Systems, Murray Hill, NJ. He joined Purdue Univ. in 2004. Dr. Alam has published over 80 papers in international journals and has presented many invited and contributed talks at international conferences. He is an IEEE Fellow and received the 2006 IEEE Kiyo Tomiyasu Award for contributions to device technology for communication systems.

Alpern, Peter [2C.2; 5C.3]
Peter Alpern studied physics at the Ludwig Maximilians Univ. of Munich where he received the Dipl. Phys. with his thesis in the area of solid state physics. He changed to the Technical Univ. of Munich where he received the Ph.D. for his work in the field of low temperature phase transitions. He joined Siemens AG in 1984 where he was concerned with development and application of new analytic methods for integrated circuits. In 1987, he transferred to Siemens Semiconductor Division. From 1999 he is with Infineon Technologies where he is actively involved in the areas of reliability physics and quality problems of packaging technology and in the study of the physics of failure at the interface between chip and package.

Amusan, Oluwole A. [4B.2]
Oluwole A. Amusan received his B.S. (2003) in electrical and electronics engineering from Alabama A&M Univ. in Huntsville, AL and the M.S. (2006) in electrical engineering from Vanderbilt Univ., Nashville, TN. He is currently working on his Ph.D. in electrical engineering at Vanderbilt Univ., Nashville, TN. His research interests include microelectronic circuit analysis and design, effects of radiation on integrated circuits, specifically designing for radiation hardness, TCAD modeling of CMOS device and modeling circuit-level soft errors.

Ancarani, Valentina [MY05]
Valentina Ancarani received the degree in chemistry from the Univ. of Catania (Italy) in 1995, discussing a research thesis on surface treatments of oxide layers. In 1996 she worked with some post graduate contracts at the Univ. of Catania and at the Univ. of Pisa (Italy), working on synthesis and characterization by NMR of liquid crystals. From 1997 to 1999 he received a grant from Istituto Nazionale di Fisica della Materia (INFM) working on the study of low-Tc superconductors. In 1999 she joined the Central R&D Group of STM in Catania working on technology development of non-volatile memories. Her current interests are technology development of advanced memory devices. She is author or co-author of several scientific papers on international reviews.

Ang, D.S. [3B.4; DI04; TR05]
D.S. Ang received the B.Eng. (hons) and the Ph.D. in electrical engineering from the National Univ. of Singapore. He is presently an assistant professor in the School of Electrical and Electronic Engineering, Nanyang Technological Univ., Singapore. His research interests include bias-temperature instability, reliability physics and characterization of advanced CMOS and novel devices. His work has been documented in more than 28 papers in the IEEE Electron Device Letters and the IEEE Transactions on Electron Devices. From 2004-2006, Dr. Ang was invited to serve on the technical sub-committees of the IRPS and the International Symposium on the Physical and Failure Analysis of Integrated Circuits.

Ang, Kah-Wee [TR03]
Kah-Wee Ang received the B. Eng (first class honors) in electrical and electronic engineering from Nanyang Technological Univ., Singapore, and the S.M. in advanced materials for micro and nano systems from Singapore-MIT-Alliance (SMA). He is currently pursuing the Ph.D. in electrical engineering at the National Univ. of Singapore (NUS). His current research involves sub-50 nm thin body silicon-on-insulator MOS transistor design and fabrication, process integration of strained channel transistors with lattice-mismatched source/drain stressors, and carrier transport characterization of nano-scale devices.

Angyal, Matt [5D.2]
Matt Angyal received his B.S. in electrical engineering from the Univ. of Maryland (1991) and his Ph.D. in electrical engineering from Cornell Univ. (1996). From 1996 through 2001 he worked at Motorola's Advanced Products R&D Lab where he contributed to the development of copper interconnect technology. He joined the IBM Semiconductor R&D Center in 2001, where he has been involved in copper / low-k interconnect technology development for advanced CMOS logic technologies.

Arnaud, Lucille [IT05]
Lucile Arnaud graduated from Institut National des Sciences Appliquées of Lyon in 1981, obtained her Ph.D. (1984) in material sciences from Université Joseph Fourier of Grenoble. She joined CEA-LETI in 1984. During the years 1984-1991, she worked on the design and characterization of solid state magnetic memories. Her main interests included electrical properties, mechanical issues and magneto-optical effects. During the years 1991-1995, she worked on high frequency characterization of passive components made with superconductors. Since 1995, she worked on interconnect reliability physics. Her main research activities covered DC and pulsed DC electromigration in Al alloys and damascene Cu as well as mechanical stress

related phenomena. Since 2001, she has been involved as project leader of European project dedicated to interconnects with Cu and ultra low k dielectrics for CMOS technology. During her carrier, she has been author or co-author of numerous technical papers and communications or invited presentations in international conferences related to the above fields.

Asao, Yoshiaki [MY01]
Yoshiaki Asao received the B.S. (1986) and M.S. (1988) in electrical engineering from Osaka Univ., Osaka, Japan. In 1988, he joined Toshiba Corp. as a device engineer in the Semiconductor Device Engineering Lab and worked on DRAM. Since 2000, He has been worked on MRAM. He is currently manager of MRAM integration technology at the advanced memory device technology department in the center for semiconductor research and development.

Asayama, Kyoichiro [FA06]
Kyoichiro Asayama received B.S. (1981) and M.S. (1983) degrees in physics from Osaka Univ., Osaka, Japan. From 1983 to 1999, he was been engaged in development of process and device technology of DRAM and SRAM. Since 2000, he has been managed by the side the Failure analysis technology group and engaged in development of TEM & STEM technology.

Aubel, Oliver [IT11; 5D.2]
Oliver Aubel received his Ph.D. (2004) in electrical engineering from Univ. of Hannover (Germany) with focus on highly accelerated electromigration lifetime testing. He is currently working for the Quality and Reliability department of AMD Saxony LLC (Germany). His main field of interest is Back End of Line reliability investigation with respect to integration processes.

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Nor Azilah received B.Eng in electrical and electronic engineering from Univ. of Salford of United Kingdom (1999). She has been employed by Silterra(M) since 2000. Her activities include fault isolation and physical device failure analysis for various device technologies.

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Yoshie Azuma received B.S.(1980) in chemistry from Yamagata Univ., Yamagata, Japan. and M.S.(1982) in chemistry from Ocyanomizu Univ., Tokyo, Japan. Since 2003, she has been engaged in applications of Nano-Prober for failure analysis of integrated circuits.

Bafleur, Marise [EL11]
Marise Bafleur received the Engineer Degree in solid state physics (1979) from the Institut National des Sciences Appliquées of Toulouse, France and the Ph.D. (1982) and the State Doctorate (1987), from Paul Sabatier Univ., Toulouse, France. During her Ph.D. thesis (1979-1982), she worked on defect characterization of molecular beam epitaxy grown GaAs layers. Since 1983, she joined the Centre National de la Recherche Scientifique (C.N.R.S.) at the Laboratoire d'Analyse et d'Architecture des Systèmes (L.A.A.S.) in Toulouse, France. From 1983 to 1987, she devoted her research activities to CMOS digital circuit design and modelling of its dynamic behavior. From 1987 to 1994, she oriented her activity towards smart power IC's design and technology. From 1994 to 1997, she spent 3 years with Motorola in Phoenix (USA), first as a low power designer and second working on TCAD predictive engineering. Since the end of 1997, she is at L.A.A.S. research institute leading a research activity in the field of Electrostatic Discharge (ESD) in CMOS and smart power technologies.

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Anupama Balasubramanian received the B.E. in electrical and electronics engineering from Birla Institute of Technology and Science, Pilani, India, (2002) and the M.S. in electrical engineering from Vanderbilt Univ., Nashville, TN (2004). She is currently working on her Ph.D. in electrical engineering at Vanderbilt Univ., Nashville, TN. Her research interests include biological sensors, microelectronic circuit analysis and design, effects of radiation on integrated circuits, specifically designing for radiation hardness and modeling circuit-level soft errors.

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N. Balasubramanian received his Ph.D. in physics from Indian Institute of Technology, Madras, India. He was an Engineering Section Manager for front end process modules with Chartered Semiconductor Manufacturing Ltd., Singapore. In 1998, he joined the Institute of Microelectronics, Singapore, where he is currently a Senior Technical Manager with the Semiconductor Process Technology Lab. He is the author/co-author of over 60 publications in peer-reviewed journals and holds 7 US patents. His current research interest include nanoscale Si devices, Si nanowire and their applications in sensors.

Banerjee, Kaustav [EL12]
Kaustav Banerjee is an Associate Professor of Electrical and Computer Engineering at the Univ. of CA-Santa Barbara. After receiving his Ph.D. in electrical engineering and computer sciences from UC Berkeley (1999), he was with Stanford Univ. as a Research Associate at the Center for Integrated Systems. In 2002 he joined the ECE faculty at UCSB, where he currently directs the Nanoelectronics Research Lab. His present research interests focus on nanometer scale issues in high-performance/low-power VLSI as well as on circuits and systems issues in emerging nanoelectronics. His research has been chronicled in over 130 journal and refereed international conference papers. He has also co-edited a book titled "*Emerging Nanoelectronics: Life with and after CMOS*" by Springer in 2004. Dr. Banerjee has been recognized through many awards and honours including the ACM SIGDA Outstanding New Faculty Award (2004) and a Best Paper Award at the Design Automation Conference (2001). He has served on the technical program committees of several leading IEEE and ACM conferences including IEDM, DAC, ICCAD and IRPS. At present, he serves as a member of the Nanotechnology Committee of the IEEE Electron Devices Society. More information about his research is available at www.ece.ucsb.edu/faculty/banerjee

Barnett, Joel [PI02]
Joel Barnett received his B.S. in chemical engineering from the Univ. of CA-Berkeley (1984) and has over 20 years of semiconductor experience. He has authored and co-authored more than 50 journal and conference papers in various semiconductor research areas including metal deposition, cleans, high-k and metal gate processes, and statistics. In 1999 he rejoined Sematech where he is a Senior Member of the Technical Staff in the Front End Processes Division. He is currently working on the High-k gate team developing pre-gate clean, post-gate etch clean and metal wet etch process solutions. He also co-chairs the ITRS Surface Preparation Sub-TWG team.

Bauwens, Filip [5C.4]
Filip Bauwens holds a M.Sc. in applied physics from the Univ. of Gent, Belgium (1995). In 2000, he received a Ph.D. in nuclear physics from the same university. In 2001, he started his career in microelectronics when joining AMI Semiconductor, Oudenaarde, Belgium. He is mainly involved in the prestudy of new smart power technologies, including process specification, assessment of electrical and degradation behaviour, and detailed TCAD studies. He is author or co-author of over 20 international journal papers or conference proceedings.

Baze, Mark P. [4B.2]
Mark P. Baze received his B.S. in physics in 1975 from Washington State Univ.. He joined the Boeing Company, first as an intern in 1974 and later on after graduation as a full time employee with the Boeing's Physics Technology Group at the Boeing Radiation Effects Lab. In 1987, he moved to the Boeing High Technology Center and later joined the Solid State Electronics Development organization in 1991. His work at Boeing has included radiation shield design, hardness assurance testing, development of laser simulation techniques for dose rate effects, total dose effects studies, single event modeling for large scale circuits, and single event effects hardening. He currently works in Boeing's Solid-State Electronics Development organization, specializing in microelectronic radiation effects modeling, hardening, and test structure design.

Beaudoin ,Felix [6A.4]
Felix Beaudoin received the Ph.D. (2002) in electrical engineering from Bordeaux Univ., Bordeaux, France. He joined Credence in 2006 as an application engineer. He is in charge of IC static and dynamic laser stimulation techniques for failure analysis and design debug of ICs. He is currently president of the European Failure Analysis Network (EUFANET) association.

Benedetti, Mattia [5B.1]
Mattia Benedetti received the degree in electronics engineering (2006) at the Univ. of Padova working on characterization and reliability of GaN ohmic contacts.

Bentz, Daniel N. [IT09]
Daniel N. Bentz received the Ph.D. (2003) in materials science and engineering, and M.S. (1999) in physics, both at Univ. of Arizona, Tucson, studied solidification of behavior of faceted and non-faceted crystal growth systems with kinetic Monte Carlo modeling at the Univ. of Arizona. After receiving his Ph.D., Daniel has held postdoctoral research appointments at Rutgers Univ. in the Dept. of Ceramics and Materials Science, where he conducted molecular dynamic simulations of silica incorporating partial charges, and at Rensselaer Polytechnic Institute at the Focus Center, New York, Rensselaer, Interconnects for Hyperintergation, were he examined thermally induced stresses in copper inter-wafer structures. At Rensselaer he also has aided in the development of grain continuum modeling of interconnect structures for intergraded circuits using Comsol Multiphysics. Dr. Bentz has joined Enig Associates, Inc. in January 2007.

Bernstein, Joseph B. [5B.2; Tut]
Joseph B. Bernstein is an Associate Professor of Reliability Engineering in the Dept. of Mechanical Engineering at the Univ. of Maryland, College Park with appointments in Electrical Engineering and the Institute for Research in Electronics and Applied Physics. He received his Ph.D. in Electrical Engineering from MIT in 1990 and he is actively involved in several areas of microelectronics reliability and physics of failure research including power device reliability, gate oxide integrity, radiation effects, MEMS and laser programmable metal interconnect. He supervises the lab for laser processing of microelectronic devices and is the head of the microelectronics device reliability program. Research areas include thermal, mechanical, and electrical interactions of failure mechanisms of ULSI devices. He also works extensively with the semiconductor industry on projects relating to laser processing for defect avoidance, programmable devices and repair in microelectronic circuits and packaging. Professor Bernstein was a Fulbright Senior Researcher/Lecturer and set up a joint center for reliable electronics at Tel Aviv and Bar Ilan Universities in Israel.

Bersuker, Gennadi [2A.4; 2A.7; 4D.3]
Gennadi Bersuker completed his M.S. and Ph.D. in physics at the Leningrad State Univ. and Kishinev State Univ., respectively. After graduation, he joined Moldavian Academy of Sciences, and then worked at Leiden Univ. (The Netherlands) and the UT at Austin. Since 1994, he has been working at Sematech on process induced charging damage, electrical characterization of Cu/low-k interconnect, high-k gate stacks and advanced CMOS process development.

Bez, Roberto [6B.1]
Roberto Bez received the doctor degree in physics at the Univ. of Milan in 1985. In 1987 he joined the Central R&D department of STM and started to work on Non-Volatile Memory (NVM) technologies. In the 90s he participated in the development the NOR Flash memory technology, in a first phase as expert of the device physics and reliability and in the second phase as project leader of the multilevel product development. In 2000 he started to investigate new NVM technologies, alternative to the floating-gate based Flash. Since 2001 he has been working on the development of Phase Change Memory technology. Currently he is the high density and emerging memories director, in the NVM Technology Development of the Front-end Technology and Manufacturing group. He has authored many papers, conference contributions and patents on topics related to NVM. He has been lecturer in Electron Device Physics at the Univ. of Milan and in Non-Volatile Memory Devices at the Univ. of Padova, Polytechnic of Milan and Univ. of Udine.

Bhuva, Bharat L. [4B.2; 4B.4; SE01]
Bharat L Bhuva received the B.S. (1982) in electrical engineering from Maharaja Sayajirao Univ. of Baroda, Baroda, India, and the M.S. (1984) and Ph.D. (1987) in electrical engineering from NC State Univ., Raleigh. He is currently an Associate Professor of Electrical Engineering with the Dept. of Electrical Engineering and Computer Science, Vanderbilt Univ., Nashville, TN. His research interests include optical signal transmission using all Si processes, biosensors, radiation effects on electronics, and cognitive science.

Billman, Curtis [2E.3]
Curtis Billman graduate research focused on interlevel dielectric reliability and the electrical characterization of crystalline semiconductor interfaces for alternative gate dielectric applications. He received his M.S. in engineering science and will receive his Ph.D. in materials science from Penn State Univ. in May 2007. He currently works at AMI Semiconductor in Quality and Reliability.

Black, Bill [2B.1]
Bill Black received an AAS (1988) and BAS (2000) in electronic engineering technology from ITT Technical Institute of Boise, ID. He joined Micron Technology in 1989 and has spent the past eighteen years working in QRA, primarily focusing on CMOS process reliability issues. Over the last couple of years he has been involved with radiation effects in semiconductors. He has coauthored several technical papers relating to CMOS reliability.

Black, Jeffrey D. [4B.2; SE01]
Jeffrey D Black is a Senior Research Engineer in the Institute for Space and Defense Electronics (ISDE) at Vanderbilt Univ.. He received his BSEE at the United States Air Force Academy in 1988 and his MSEE at the Univ. of New Mexico in 1991. He is current pursuing his Ph.D. at Vanderbilt Univ.. His areas of specialty and interest are single event effects and mitigation approaches. Prior to joining ISDE in 2004, he worked for Mission Research Corp. in Albuquerque, NM. He just completed serving a three year term as Secretary of the Radiation Effects Steering Group for IEEE NPSS.

Bloomfield, Max O. [IT09]
Max Bloomfield is a doctoral candidate in the Dept. of Chemical and Biological Engineering at Rensselaer Polytechnic Institute, where he has been worked for the Focus Center - New York, Rensselaer; Interconnections for Hyperintegration. His doctoral work focuses on developing novel computational techniques for tracking interfaces in many-phase systems, which he has incorporated into a parallel software framework, called PLENTE. These techniques have direct application to simulations of microstructure, radiological dosing, and multi-phase fluid flow, to name a few. Max holds a degree in chemistry from the State Univ. of New York at Albany.

Boit, Christian [6A.3]
Christian Boit is chair of semiconductor devices in Berlin Univ. of Technology (Germany). There, he received the diploma in physics and the Ph.D. in electrical engineering. He joined Siemens research labs 1986 in Munich as a pioneer of photon emission. He was part of IBM-Siemens 64M DRAM project in East Fishkill NY. Later he was Director of Failure Analysis at Infineon Technologies. He has been co-founder of EDFAS and the European Failure Analysis Network EUFANET. In 2002, he has been General Chair of ISTFA. Currently, Chris serves as Vice President in EDFAS.

Bolom, Tibor [5D.2]
Tibor Bolom received his Ph.D. (2000) in material science from Technical Univ. of Munich (Germany). Currently he works as a Process Dev Engineer at ASTA/IBM Metal module for AMD, Inc. His main field of work is the process development of PVD/ALD Metallization including Barrier/Seed and CA Liner/Fill materials.

Boselli, Gianluca [4C.3]
Gianluca Boselli completed his master's studies in electrical engineering at the Univ. of Parma, Italy, in 1996. In 2001 he completed his doctoral studies at the Univ. of Twente, The Netherlands, where he worked on high current phenomena of CMOS components. In 2001, he joined the Silicon Technology Development group of Texas Instruments, Dallas, Texas, USA. Since joining Texas Instruments, his work focused on ESD and Latch-up development for advanced CMOS technologies with special emphasis on process and modeling aspects. He authored and co-authored several papers in the area of ESD and Latch-up. He presented his work at major conferences, including IEDM, IRPS and EOS/ESD Symposium. He also presented invited papers and/or tutorials at the EOS/ESD Symposium, IRPS, IEDM, ESREF and RCJ. Dr. Boselli has been the recipient of the Best Paper Award on behalf of Microelectronics Reliability Journal in 2000. He received The Best Paper Award at the EOS/ESD Symposium 2002. He also received the The Best Presentation Award at the EOS/ESD Symposium in 2002 and in 2006. Dr. Boselli is a senior member of IEEE and a member of ESD Association. Dr. Boselli serves on the Technical Program Committee of the EOS/ESD Symposium, IRPS and ESREF. Dr. Boselli has served as Technical Program Chair at the EOS/ESD Symposium 2006 and will serve as Vice-General Chair at the EOS/ESD Symposium 2007.

Bottini, Roberta [DI06]
Roberta Bottini graduated in physics from the Univ. of Milano, Italy, (1991). In 1993 she joined the STM in Agrate Brianza (Italy) working in the Non-Volatile Memory Process Development group within the Central R&D, where she worked till 1995 on MOSFET electrical characterization and from 1995 to 2000 on process integration and EEPROM FLASH memory reliability. In 2000

she joined the Dielectric Reliability group. She has published more than 10 technical papers in international journals and conferences and has several patents on the above mentioned topics.

Boulanger, Fabien [2A.6]
Fabien Boulanger graduated and then received a Ph.D. (1991) from the Ecole Centrale de Paris in energetics. He joined the CEA to work on model and software development in thermal hydraulics for nuclear safety studies. He was then manager of the lab of advanced software development on this topic. He joined then the CEA-LETI and is now the manager of the lab dedicated to numerical simulation and electrical characterization of CMOS process and devices.

Bouyssou, Emilien [5A.1]
Emilien Bouyssou received the M.S. (2002) from the Graduate School of Physics and Chemistry of Bordeaux (ENSCPB), and the Ph.D. (2006) in electronics from the Univ. of Tours. He is currently working at STM, Tours, France, in R&D department. His main research interests are focused on Device Characterization and Reliability issues, and more especially on dielectric breakdown.

Bowen, Chris [3B.1]
Chris Bowen received the B.S. in electrical engineering from the Georgia Institute of Technology (1988), and the M.S. (1992) and Ph.D. (1995) in electrical engineering from the UT at Dallas. His dissertation focused on full-band quantum transport and this work was incorporated into the NEMO quantum device simulation tool. From 1989 to 1993, he was a device engineer at Texas Instruments (TI) Incorporated, Dallas, working on analog and mixed signal technologies. From 1996 to 1998, he was with the Semiconductor Process Development Center, TI, where he performed long-rage research on sub-50nm metal gate CMOS. From 1998 to 2000, he was a Senior Scientist at the Jet Propulsion Lab, where he developed NEMO-3D, a simulator that computes strain field, quantum states, and optical matrix elements in multimillion atom systems using tight-binding Hamiltonians. He is currently a Senior Member of the Technical Staff at the Silicon Technology Development Group, TI, where he has applied atomistic-based quantum transport simulation to engineer transistor performance enhancement in advanced CMOS technologies. He has authored or coauthored over 50 refereed articles.

Brambilla, Marzio [DI06]
Marzio Brambilla, chemist, joined the STM in Agrate Brianza (Italy) in 1974 working on epitaxy for ten years and since 1989 he is responsible of SEM characterization and failure analysis in the Physics group in Central R&D.

Brazzelli, Daniela [DI06]
Daniela Brazzelli graduated in physics from the Univ. of Milan (1998). She joined STM in 1999 and she is currently working in the Non-Volatile Memory Process Development group within the Central R&D Dept.. Her research activities include failure and wear-out mechanisms of thin active dielectrics. She has published more than 10 technical papers in international journals and conferences.

Brisbin, Douglas [5C.5]
Douglas Brisbin received his B.S. from Miami Univ., M.S. and Ph.D. in Physics from Kent State Univ.. He joined National Semiconductor in 2001 and is currently working as Principal Device Reliability Engineer in the Advanced Process Technology Development group. His interests are in the area of MOS/bipolar hot-carrier degradation, ultra-thin gate oxide integrity and NBTI. He is an active member of the JEDEC 14.2 Wafer Level Reliability Standards Committee and contributed to more than twenty technical publications.

Bruynseraede, Christophe [IT08]
Christophe Bruynseraede received the M.S. in electrical engineering (1993) and the Ph.D. (2000), both from the Katholieke Universiteit Leuven, Leuven, Belgium. He is currently continuing his research at the Interuniversity Microelectronics Center (IMEC), whereby his main research interests are focused on reliability issues (electro-and stressmigration) in advanced Cu/low-k interconnects. He has authored and co-authored over 35 papers and conference contributions in the fields of opto-electronics, magneto-electronics and BEOL reliability.

Budiman, Arief Suriadi [2D.2]
Arief Suriadi Budiman received his B.S. in mechanical engineering from Institute of Technology, Bandung (ITB), Indonesia (1995), and his M.EngSc in materials engineering from Monash Univ., Australia (1998). He then embarked on his technical career with Hewlett-Packard, Co in Singapore researching and developing microfabrication processes for HP's latest generation of inkjet print head MEMS chip. During this time, he patented two U.S Patents on electrical interconnects for an inkjet die and filed one on thermal inkjet micro-mixer for biomedical purposes. Currently beginning his 5th year in his Ph.D candidacy at Stanford's Dept. of Materials Science & Engineering under the supervision of Prof. Bill Nix (William D. Nix), Mr. Budiman is completing his dissertation and will graduate in Summer 2007. At the core of his research is the study of mechanics of materials at the nanoscales (nanomechanics). At Lawrence Berkeley Lab, he uses the synchrotron x-ray diffraction as a nanoprobe to look at crystalline materials and its evolution during deformation. The results of Mr. Budiman's new nanoscale probing capability have unveiled important fundamental knowledge, as well as very practical implications to the electromigration reliability community in the Cu interconnect industry. For this research, Mr. Budiman has just been awarded with the Materials Research Society (MRS) Graduate Student Award in Boston, MA, in November 2006. He gave two symposium invited talks in the MRS spring and fall meetings in 2006 on these topics. He has won several other awards as well for innovations, best student and best papers.

Butler, David L. [DI01]
David L. Butler received a B.S.(1998) and M.S.E. (2005) in electrical engineering from Boise State Univ.. In 1998, he joined Micron Technology and is currently responsible for the qualification of new devices, reliability studies, and failure analysis for DRAM products.

Bychikhin, Sergey [EL10]
Sergey Bychikhin received his MSc (1995) and Ph.D. (2000) from Physics department of the M.V.Lomonosov Moscow State Univ., Russia. Since 2000 he joined the group for semiconductor device characterization in the Institute for Solid State Electronics in Vienna where he is engaged in the field of the thermal and free carrier analysis of the ESD protection structures by backside laser interferometry. His current research interests are in the device characterization and simulation during the HBM and CDM stress.

Byun, Hyeong-Jik [2C.4]
Hyeong-Jik Byun received B.S. (1987) in computer science from Daegu Technical College. He has been at Samsung since 1992 as a reliability failure analysis engineer. His main interest is to develop new accelerated test methods for reliability evaluation.

Cale, Timothy S. [IT09]
Timothy S. Cale is a Professor of Chemical and Biological Engineering at Rensselaer Polytechnic Institute. Professor Cale received his Ph.D. in chemical engineering from the Univ. of Houston (1980). Professor Cale's research focuses on transport and reaction fundamentals; most recently for processes used to fabricate integrated circuits. He developed a widely used 'ballistic' transport and reaction model applicable to low pressure deposition and etch processes. This model has been used in several computer programs to understand how process conditions affect thin film processing at the feature (sub-micron scale). He has demonstrated the linking of equipment scale and feature scale models in concurrent/single multiscale process simulations. He has proposed and successfully demonstrated processes in which process conditions are varied in a preprogrammed, model driven manner to optimize process or film properties. He currently focuses on simulations designed to understand microstructure formation and evolution in polycrystalline materials, with a goal to predict product relevant performance of thin films.

Campbell, Jason P. [5D.1]
Jason P. Campbell received his B.S. in engineering science from Penn State Univ. (2001). He is currently pursuing his Ph.D. in engineering science from Penn State Univ.. His current research involves the atomic scale mechanisms responsible for NBTI.

Carbonell, Laureen [4E.4]
Laureen Carbonell received her diploma in chemistry at the Ecole Nationale Supérieure de Chimie de Toulouse (ENSCT) in France. From 1997 until 2000 she carried out her Ph. D. in materials science at the Laboratoire de Minéralogie-Cristallographie de Paris (LMCP) in France focusing on the epitaxial growth and characterization of ferromagnetic layers onto ZnSe based semiconductors. Since 2000, she has joined the Interuniversity Microelectronics Center (IMEC) in Belgium, where her R&D activity has been focusing on copper electroplating

in sub-100 nm interconnects. She has authored and co-authored more than 40 publications.

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Amitabh Chatterjee graduated from IIT Powai with (5yrs Int.) M.Tech in electrical engineering and subsequently, he joined as a scientist at the Centre for Advanced Technology, Indore in the Laser Physics Division in 1996. His work involved development of ultra fast avalanche transistor based HV Marx Bank Circuit ands its impact on the stability of ultra-short laser pulses. His research included analysis of bipolar snapback due to low doped resistive drift region of a HV BJT under avalanche break-down and study of avalanche injection mechanisms from the ohmic contacts. Currently he is working on his doctoral dissertation on the reliability of Drain Extended NMOS (DeNMOS) under ESD stressing at the Univ. Of CA, Santa Barbara.

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2002 to 2003, he researched about high-k dielectrics integrating into flash memory as a visiting researcher in the UT at Austin. Currently, as a vice president in semiconductor R & D center, he is responsible for flash cell transistor development and process integration of the next generation flash memory. He holds more than 30 international patents related to non-volatile memory circuit, device structure and fabrication method, and has authored and coauthored more than 15 technical papers in international conferences and journals. In addition, he has served on the technical committee of Non-Volatile Semiconductor Memory Workshop (NVSMW) since 2004.

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James Demarest received his B.S. (1996) in materials science and engineering from Lehigh Univ.. He then continued his studies at the Univ. of Virginia and graduated (2001) with a Ph.D. in materials science and engineering. While at UVA, his principle interests lay with transmission electron microscopy of semiconductor devices and materials along with focused ion beam microscopy and scanning electron microscopy. He then joined IBM in 2001, and began performing reliability failure analysis on developing technologies. His interests currently include all aspects of reliability failure analysis including defect isolation, low-k and ultra low-k dielectric materials, metallization reliability stressing, and chip-package interactions.

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Rainer Duschl received the diploma degree in physics (1997) from the Univ. of Regensburg and the Ph.D. (2000) from the Max Planck Institute for Solid State Research in Stuttgart. In 2000, he joined Infineon Technologies AG, Technology Development in Munich, Germany, working on process integration of BiCMOS technologies. Since 2002 he is engaged in reliability of CMOS gate oxides and dielectrics in memory, CMOS and power technologies.

Dutton, Robert W. [2B.2]
Robert W. Dutton is Professor of Electrical Engineering at Stanford Univ. and director of Research in the Center for Integrated systems. He received the B.S. (1966), M.S. (1967), and Ph.D. (1970) from the UC, Berkeley. He has held summer staff positions at Fairchild, Bell Telephone Labs, Hewlett-Packard, IBM Research, and Matsushita. His research interests focus on Integrated Circuit process, device, and circuit technologies—especially the use of Computer-Aided Design (CAD) in device scaling and for RF applications. Dr. Dutton has published more than 200 journal articles and graduated more than four dozen doctorate students. He was Editor of the IEEE CAD Journal (1984-1986), winner of the 1987 IEEE J. J. Ebers and 1996 Jack Morton Awards, 1988 Guggenheim Fellowship to study in Japan, was elected to the National Academy of Engineering in 1991, honored with the C&C Prize (Japan) in 2000, and received Career Achievement Award (2005) from the Semiconductor Industry Association (SIA) for sustained contributions in support of research that is critical to SIA needs. Most recently, he received the Phil Kaufman Award.

Duvvury, Charvaka [4C.3; EL12]
Charvaka Duvvury is a Texas Instruments Fellow working in the Silicon Technology Development Group at Dallas. He received his Ph.D. in engineering science from the Univ. of Toledo. He has published over 100 papers in ESD and other IC reliability topics, co-authored four books, and holds more than 55 patents. Charvaka has been with TI for more than 25 years and worked on DRAM circuit design, transistor modeling, and hot carrier reliability before exclusively focusing on ESD development starting from the 1 μm technologies. He is currently supporting ESD development for advanced nanometer technologies and is a corporate consultant on many product ESD issues. He has made several international presentations on ESD at various conferences and universities. He has been involved with the ESD Symposium since 1984, having served as the Technical Program Chair in 1992 and as the General Chair twice in1994 and 2005. He has received the Outstanding Contributions Award and numerous Best Paper Awards from the ESD Symposium. He is a member of the ESDA Board of Directors since 1997, promoting university research and education in ESD. He is also a Fellow of the IEEE.

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Yoshiyuki Eto a graduate of Nihon Univ. with a degree of physics. He began his career at JEOL in 1995, as a research and development engineer, mainly engaging in the development fields of semiconductor inspection systems and their applications, such as bare and patterned wafer review SEMs, edge inspection and defect classification.

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Pascal Fouillat received the M.S. (1980) in electronics from the Ecole Normale Supérieure de Cachan, France, and the Ph.D. (1990) from the Univ. of Bordeaux 1, France. Since 1997, he has been a full professor at the Ecole Nationale Superieure d'Electronique, d'Informatique et de Radiocommunication de Bordeaux, France, and in IXL, the microelectronics lab at the Univ. of Bordeaux 1. In 1998, he took the head of the Design and Test Group, IXL. He's now the Director of the IMS Lab. His research interests are in IC design, space electronics and non-destructive test of ICs using a laser beam.

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Thomas Fu received his Ph.D. in electrical and electronics (1989) from State Univ. of New York at Buffalo, NY. He was working at Texas Instrument Semiconductor Process Design Center for 6 years; thereafter as a Fab Manager at Power Chip Semiconductor Corp. and Vanguard International Semiconductor for 5 and 3 years respectively. Currently, he is the Vice President of Technology Development department with Chartered Semiconductor Manufacturing Ltd., Singapore.

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Shinji Fujieda received B.S. (1982) and M.S. (1984) in applied physics from Univ. of Tokyo, and the degree of Dr. Eng. (2004) from Tokyo Metropolitan Univ.. In 1984, he joined NEC Corp., Japan, where he was engaged in the research of process technology for compound semiconductor devices. He is recently working on high-k gate stacks and embedded non-volatile memories in System Devices Research Labs of NEC.

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Nadia Galbiati graduated in physics from the Univ. of Milano Italy, (1994) and obtained a master 's in material science (1997) from the Univ. of Milano, Italy. In 1998 she joined the STM in Agrate Brianza (Italy) working in the Non-Volatile Memory Process Development group within the Dielectric Reliability group of Central R&D. Her research activities include failure and wear-out mechanism of all active dielectric of Eprom, Flash EEprom and E2Prom devices and the evaluation of new technologies for the future generations.

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Jeff Gambion received the B.S. (1979) in materials science from Cornell Univ., Ithaca, NY, and the Ph.D. (1984) in materials science from the Massachusetts Institute of Technology, Cambridge, MA. He joined IBM, Hopewell Junction, NY, in 1984, where he worked on silicide processes for Bipolar and CMOS devices. In 1992, he joined the DRAM development alliance at IBM's Advanced Semiconductor Technology Center, Hopewell Junction, NY. While there, he developed contact and interconnect processes for 0.25-, 0.175-, and 0.15-mm DRAM products. In 1999, he joined IBM's manufacturing organization in Essex Junction, VT, where he has worked on copper interconnect processes for CMOS logic and CMOS imager technology. He has published over 90 technical papers and holds over 100 patents.

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Gan Chee Lip is currently an assistant professor in the School of Materials Science and Engineering, Nanyang Technological Univ., Singapore and a SMA Fellow in the Advanced Materials for Micro- and Nano-Systems under the Singapore-MIT Alliance (SMA) Program. His current research interests include the reliability study of advanced interconnect systems, such as copper electromigration, TDDB of low-k dielectrics, as well as the process integration and reliability of 3D interconnects through copper-copper wafer bonding. He is also in the executive committee of IEEE Singapore Rel/ED/CPMT Chapter.

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Wolfgang Goes studied technical physics at the TU Wien, where he received the degree of Diplomingenieur in 2005. He joined the Institute for Microelectronics in January 2006, where he is currently working on his doctoral degree. His current scientific interests include abinitio and moleculardynamics simulations as well as the NBTI phenomenon.

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Xavier Garros received the M.S. in physics engineering, from the National Polytechnics Institute of Grenoble, France (2000) and his Ph.D. from the Univ. of Marseille, France (2004), on the physics and electrical properties of High-K dielectrics as the replacement of SiO_2 for the future CMOS technologies. Now he's working in CEA/Leti on the reliability of High-k oxides.

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Gerardi, Cosimo [MY05]
Cosimo Gerardi received the degree cum laude in solid state physics in 1989 from the Univ. of Lecce (Italy). From 1990 to 1992 he was at the Dept. of Physics of the Univ. of Padua (Italy), where he developed his skill on surface analysis techniques focusing on SIMS and RBS. From 1992 to 1997 he was at the Centro Nazionale Ricerca e Sviluppo dei Materiali (CNRSM) of Brindisi (Italy), first as a researcher and then as senior researcher responsible for surface analysis of semiconductors by using SIMS, XPS and Auger spectroscopy. He worked mainly on the analysis of SiGe, III-V and II-VI heterostructures, superlattices and quantum wells developing analytical methodology combining SIMS, XPS, XRD and TEM. In 1997 he joined the Central R&D Group of STM in Catania (Italy) with the charge of senior researcher and then as manager of the device engineering section. His fields of interest are focused on state-of-the-art and advanced non volatile memories with particular focus on technology development and electrical characterization. He is author and co-author of more than 120 papers and several international patents.

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Andrea Ghetti received the laurea degree (1994) and the Ph.D. (1998) in electrical engineering both from the Univ. of Bologna, Bologna, Italy. In 1994 he was visiting scientist at the TCAD department of Intel Corp., Santa Clara, CA, for three months. From 1997 to 2000 he held a post-doctoral position at Lucent Technologies, Bell Labs, Murray Hill, NJ. In 2000 he joined STM, Agrate Brianza, Italy. His research interests are in the field of non-volatile memory development and device modeling, simulation and characterization with particular regard to 3D effects, Monte Carlo simulation, quantum phenomena, mechanical stress, hot carrier, tunneling in MOS structures and oxide reliability.

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Gabriella Ghidini graduated in physics from the Univ. of Parma, Italy, (1979) and received the Ph.D. in physics (1983) from the City College of New York. In 1983 she joined the STM in Agrate Brianza (Italy) working in the Physics group of the Central R&D department. In 1987 she moved to the Non-Volatile Memory Process Development group within the Central R&D, becoming the leader of the Dielectric Reliability group. Her research activities include failure and wear-out mechanism of all dielectrics of Flash NOR, NAND , Flash EEprom and E2Prom devices and the evaluation of new technologies for the future generations. She is coauthored over 100 papers published in journals or presented in international conferences and six patents on the above mentioned topics.

Gieser, Horst A. [4C.1]
Horst A. Gieser has graduated in electrical engineering at the Technical Univ. of Munich TUM. In 1999 he received his Dr.-Ing. title for the characterization of integrated structures with very short high-current pulses and studies on CDM. In 1989 he founded the Lab for Analysis and Test of Integrated Systems ATIS at the TUM Chair for Integrated Circuits. ATIS is now a department of the Fraunhofer Institute for Reliability and Microintegration IZM. The ATIS department, located in Munich, is dedicated to research, consulting services and lecturing. Horst is a founding member and currently the president of the ESD-FORUM e.V. association. He received the Best Paper Award of the EOS/ESD-Symposium 1996 and of EOS/ESD-Symposium 1993 as a co-author. He co-authored the ESREF Best Poster Papers 1993 and 1995 and will be TPC Chair of the 2007 EOS/ESD-Symposium. Horst received the Fraunhofer IZM-Research Award 2001 for outstanding research contributions in the field of electrostatic discharge and pulsed high-current characterization. He has published more than 50 papers and patents, the majority of them in the field of ESD and Vertical System Integration VSI. He has contributed to the second edition of the book ESD in Silicon Devices edited by A. Amerasekera and C. Duvvury. His future research interest will extend into the field of cost effective test solutions for system integration, high frequency characterization and modelling of SiGe devices and the test of circuits of polymeric devices and in flexible, ultra-thin semiconductor substrates.

Gill, Jason [5D.2]
Jason Gill received his B.A. in physics and mathematics from Skidmore College (1995), and his M.S. in mechanical engineering from the Univ. of Vermont (1998). He joined IBM Microelectronics in 1996, and has been involved in technology reliability for advanced CMOS logic technologies.

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Daniel Gitlin joined Xilinx Inc. in 1992, and currently serves as vice president of semiconductor technology development. He is instrumental in driving process technology for all Xilinx products. With more than 20 years of collective experience in semiconductors, he is a member of the Technology Strategy Committee of the Semiconductor Industry Association (SIA) and has published numerous technical articles. Gitlin also holds nine patents. Gitlin received his bachelor's in engineering physics from the UAM, Mexico and graduate degrees in applied physics and electrical engineering from Harvard and UCLA, respectively.

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Bob Gleixner received his B.S. (1992) in materials science from Cornell Univ. and his M.S (1994) and Ph.D. (1998) in materials science from Stanford Univ.. His dissertation research focused on developing and validating physically-based models of electromigration and stress-induced voiding in microelectronic interconnects. He joined Intel's Quality and Reliability group in 1998, and has worked on microprocessor, microdisplay, and non-volatile memory technologies and products. Currently, Bob is with Intel's Flash Memory Group in Santa Clara, CA and is responsible for the quality and reliability of Intel's phase-change memory products.

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Neil Goldsman received the Ph.D. in electrical engineering from Cornell Univ., Ithaca, NY (1989). He is a Professor in the Electrical and Computer Engineering Dept. at the Univ. of Maryland, College Park. He is an originator of the Legendre Polynomial/Spherical Harmonic Boltzmann approach to device simulation. Recently, he has focused on mixed-signal VLSI, radio-frequency CMOS circuit design, wide-bandgap semiconductors, and nanoscale devices, including carbon nanotubes. He directs the Mixed-Signal VLSI Design Lab and the Semiconductor Device Simulation Lab at the Univ. of Maryland. His main research interests are in the areas of device, material and circuit modeling and design. He has written two educational texts in electronics used at the Univ. of Maryland, and has published more than 100 technical papers. Dr. Goldsman is the recipient of the National Science Foundation's Research Initiation Award, the Univ. of Maryland IEEE Professor of the Year Award, the George Corcoran Award for Contributions to Education, and the IEEE Benjamin Dasher Award.

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Jeng Gong received the B.S. (1975) from National Cheng Kung Univ., Taiwan, and the M.S. (1980) and Ph.D. (1983) in electrical engineering from the Univ. of Florida. He joined the Dept. of Electrical Engineering at National Tsing Hua Univ., Taiwan, in 1983, as an Associate Professor and became a professor in 1989. His research interests include noise properties in semiconductor devices, power semiconductor devices, device modeling, and device reliability.

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Tibor Grasser received the Diplomingenieur degree(1995) in communications engineering, the Ph.D. (1999) in technical sciences, and the venia docendi in microelectronics (2002) from the Technische Universität Wien. He is currently employed as an Associate Professor at the Institute for Microelectronics. Since 1997, he has headed the Minimos-NT development group, working on the successor of the highly successful MiniMOS program. He was a visiting research engineer for Hitachi Ltd., Tokyo, Japan, and for the Alpha Development Group, Compaq Computer Corp., Shrewsbury, USA. In 2003, he was appointed head of the Christian Doppler Lab for TCAD in Microelectronics, an industry-funded research group embedded in the Institute for Microelectronics. Dr. Grasser is the co-author or author of nearly 200 articles in scientific books, journals, and conferences proceedings, is the editor of a book on advanced device simulation, a senior member of IEEE, and co-chair of SISPAD 2007. His current scientific interests include circuit and device simulation, device modeling and reliability issues.

Groeseneken, Guido [2A.5;4E.4;EL11;IT08]
Guido Groeseneken received the M.Sc. in electrical and mechanical engineering (1980) and the Ph.D. in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium. In 1987 he joined the R&D Lab of IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, where he is responsible for research in reliability physics for deep submicron CMOS technologies. Since 2005 he is also responsible for the IMEC Post CMOS Nanotechnology program within IMEC's core partner research program. Since 2001 he is also Professor at the KU Leuven and since 2005 he has become an IEEE Fellow. He has made contributions to the fields of nonvolatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric breakdown of oxides, ESD-protection and testing, plasma processing induced damage, electrical characterization of semiconductors and characterization and reliability of high k dielectrics. He has served as a technical program committee member of several international scientific conferences, among which the IEDM, the European Solid State Device Research Conference (ESSDERC), the IRPS, the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM. In 2005 he was the General Chair of the Insulating Films on Semiconductor (INFOS) conference, organized in Leuven, Belgium. He has authored or co-authored more than 300 publications in international scientific journals and in international conference proceedings, 3 book chapters and 7 patents in his fields of expertise.

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Chloé Guérin received the Engineer degree in materials and microtechnologies from the Institut National des Sciences Appliquées, Toulouse, France, and the M.S. in nanophysics from Paul Sabatier Univ. of Toulouse, France, in 2005. She is currently working toward the Ph.D. in the Reliability Group of Central R&D, STM, France, in collaboration with the Laboratoire Matériaux et Microélectronique de Provence (L2MP), Toulon, France. Her research activities include device reliability and modelling.

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Moshe Gurfinkel received his B.Sc. (2003) and his M.Sc. (2005), both cum laude in electrical engineering from Tel Aviv Univ., Israel. Currently he is pursuing his Ph.D. in electrical engineering from Tel Aviv Univ., Israel. In the last year he is participating in an exchange program at the Univ. of Maryland and working as a guest researcher in the Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), Gaithersburg, MD. His research interests involve reliability and characterization of advanced microelectronic devices.

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Gaddi S. Haase received his Ph.D. in physical chemistry from the Hebrew Univ. in Jerusalem, Israel (1989). Following post-doctoral research periods in the Microelectronics Science Labs at Columbia Univ. in New York, and at the Chemistry Dept. of the Univ. of Wisconsin, Madison, he became a professor at the Chemical Physics Dept. of the Weizmann Institute of Science in Israel, in 1992. At the Weizmann Inst., Gaddi used scanning tunneling microscopy-related techniques in ultrahigh vacuum to study semiconductor surfaces. In 2001 he joined the Silicon Technology Development division at Texas Instruments, in Dallas, Texas, working on various process development projects and interconnect dielectric reliability. Gaddi is a member group technical staff, and holds a patent and 30 publications in refereed journals.

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Daniel Habersat earned his B.S. in physics from the Univ. of Maryland, College Park (2001). He is on-track to earn his M.S. in applied physics from Johns Hopkins Univ. in spring 2007. Since 2002, he has been working for the Sensors and Electron Devices Directorate at the Army Research Lab in Adelphi, MD. Mr. Habersat is currently the lead technical engineer for the MOS Evaluation Team of the Power Components Branch. His research interests are focused on the evaluation of MOS interface defects and their influences on device performance and reliability.

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Sangyeon Han received the B.S. (1993), M.S. (1997), and Ph.D. (2003) in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Taejon. From 1995 to 2003, his research interests included e-beam lithography, ultrathin radical oxide, and nanoscale CMOS devices. Mr. Han won the bronze medal of the Human-Tech Thesis Prize from Samsung Electronics Co. Ltd. And third place in the AMK paper contest from Applied Materials Korea, both in 2001. He also won second place in the IEEE Region 10 Postgraduate Student Paper Competition in 1998. In 2003, he joined Samsung Electronics, Korea, where he is currently developing DRAM process architecture for the high speed and low power product. His main research interest is the development of transistors with low threshold voltage.

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Harlan Rusty Harris received a B.S. in engineering physics (1997) and a Ph.D. in electrical engineering (2003) from Texas Tech Univ. in the area of surface and interface analysis for silicon devices. He worked on the design and construction of the semiconductor lab at the Univ. of Missouri-Columbia while teaching undergraduate classes as a Visiting Assistant Professor. Summer 2004 found Dr. Harris investigating PMOS high k reliability problems as a Visiting Scientist at Sematech before joining AMD as a Project Engineer assigned to Sematech in the area of Advanced Gate Electrodes.

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Paul Hashimoto received his B.S. in biology from Univ. of CA, Los Angeles, and in chemistry from CA State Univ., Los Angeles. He has been with Hughes for 12 years, first working at Hughes Radar Systems as a material and process engineer and is currently at HRL Lab as an Engineering Specialist with the GaN group.

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Fumihiko Hayashi received the B.S. (1988) in electrical engineering from Waseda Univ., Japan. He joined NEC Corp., Japan, in 1988, where he was engaged in the research and development of CMOS SRAMs, poly-Si thin film transistors, and Flash memories. From 1997 to 1998, he worked as Visiting Scholar at Center for Integrated Systems, Stanford Univ., CA. He is currently working on the development of embedded Flash memory technology at NEC Electronics Corp., Japan.

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Rodolf Herfst received the M.S. (2004) in applied physics from the Eindhoven Univ. of Technology, Eindhoven, The Netherlands. His master thesis was based on research done on laser cooling of iron atoms at the atom optics group of prof.dr. H.C.W. Beijerinck. He currently is a Ph.D. student at NXP Semiconductors in Eindhoven in the device modelling group of Dr. H.G.A. Huizing on the subject of RF MEMS capacitive switches. His research interests include reliability physics, modelling and characterization of RF MEMS capacitive switches.

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Hong, Kwon [FA02]
Kwon Hong received the B.S. (1989), M.S. (1992), and Ph.D. (1995) in material science and engineering from the Korea Univ., Seoul, Korea. Since 1995, he has been working at Hynix Semiconductor Inc., Korea, and has been conducting research in the area of high-k dielectric and noble metal electrode, nonvolatile memory, and reliability of DRAM capacitor. Recently his current research interests include high-k stack with silicon oxide as a interpoly dielectric for NAND Flash memory.

Hong, Sung-Joo [MY06]
Sung-Joo Hong is a Vice President of R&D Division of Hynix Semiconductor Inc. and responsible for the development of device and process integration of DRAM. Dr. Hong received the B.S. (1985) in physics from Seoul National Univ., Seoul, Korea, and the M.S. (1987) and Ph.D. (1992) in semiconductor physics from Korea Advanced Institute of Science and Technology, Seoul, Korea. He joined Hyundai Electronics Industries Co., Ltd. (currently Hynix Semiconductor Inc.) in 1992, and has been developing DRAM devices and process integration technologies. He participated in the development of 0.55μm and 0.22μm DRAM technologies as a senior member of technical staff, and led the development of 0.15μm, 90nm DRAM technologies as a technical manager, and 80nm, 66nm DRAM technologies as a director. He is now in charge of the development of 54nm and 44nm DRAM technologies and new memory technologies.

Hong, Sun-Min [MY06]
Sung-Min Hong received the B.S. (2001) in electrical engineering from Seoul National Univ., Seoul, Korea, where he is currently pursuing the Ph.D. His current research interests include noise modeling in semiconductor devices and developing a mixed-mode device-circuit noise simulation framework.

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Young Ki Hong received the B.S. (1992) in physics from Yonsei Univ., Seoul, Korea, the M.S. (1994) in physics from Yonsei Univ., Seoul, Korea, and the Ph.D. (2006) in electrical and electronic engineering from the Imperial College London, London, U.K. From 1994, he has been a member of technical staff at Semiconductor R&D Center of Samsung Electronics. His research interests are Ferro-electric device integration including PZT deposition, novel metal etching, and electrical degradation in device, especially FRAM scaling.

Hopper, Peter [EL09]
Peter received his B.Sc. in electronics from Dundee Univ., Scotland and went on to research towards Ph.D. in the Field of inertial confinement laser fusion, working with a lab in Oxford. In industry, he worked for 5 years at Inmos and SGS-Thompson in Process and Device engineering positions. He joined Silvaco International in 1990, where he started the Technology CAD integration effort and ran it as Director of Technology until 1996. He is currently the Director of Device Engineering Group at National Semiconductor.

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Kozo Katayama received the B.S. (1980), M.S. (1982) and Ph.D. (1985) in electronic engineering, from the Univ. of Tokyo, Tokyo, Japan. He joined the Central Research Lab, Hitachi Ltd., Tokyo, Japan, in 1985. He stayed at Hitachi Cambridge Lab, Hitachi Europe Ltd., Cambridge, UK, from 1997 to 1998. He moved to Semiconductor and Integrated Circuits, Hitachi Ltd. in 1999. Since that time he has been engaged in research and development of the MONOS type nonvolatile memory for embedded applications.

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Andreas Kerber received his Diploma in physics from the Univ. of Innsbruck, Austria, (2001), where he was working at Bell Labs, Lucent Technologies, Murray Hill, NJ, on the electrical characterization of ultra thin gate oxides. In 2001 he joined Infineon Technologies in Munich, Germany. From 2001 to 2003 he was assigned to International Sematech at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. At the same time he fulfilled the requirements for a Ph.D. in electrical engineering and defended his thesis

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Hyun-Ho Kim received the B.S. (1992) in material engineering from Hanyang Univ., and the M.S. (1994) and Ph.D. (1999) from Korea Advanced Institute of Science and Technology. His research topic in Ph.D. course was the development of Pb-based ferroelectric materials for FRAM and DRAM applications. In 1999, Dr. Kim joined in Technology Development Team in Samsung Electronics where he has played a major role in developing FRAM devices, such as stand-alone 4Mb and 32Mb FRAM and FRAM-embedded smart card. Dr. Kim has researched on multi-ferroic materials, especially BiFeO3, for future memory device applications in Cambridge Univ. from 2004 to 2005. His currents interests are memory-cell design, process integration, device evaluation and failure analysis of FRAM devices.

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Ulrike Kindereit received the M.S. (Dipl.-Ing.) in electrical engineering from Berlin Univ. of Technology, Germany (2005). She focused on semiconductor devices, with an internship on photovoltaics at Q-Cells and a master thesis on Laser Stimulation of Integrated Circuits, supported by Robert Bosch GmbH. Currently, she is engaged in a project with Credence DCG as a Ph.D. student. The field of research is Laser Voltage Probing (LVP) - detailed understanding of the physical origin of the LVP signals and forecasts about future scaling.

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Elizabeth Kolawa has been with the Jet Propulsion Lab, Pasadena, CA, since 1993. Presently, she is responsible for developing thermal cycle resistant electronics for the Mars focused technology program and managing the advanced measurement and detection technology program for JPL. Her research interest includes electrical contacts to semiconductors, diffusion barriers, and integration of microsystems, electronics packaging and technologies for extreme environments.

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Dimitris K. Kontos received his B.S. (2002) in physics from the Univ. of Thessaloniki, Greece and his M.S. (2005) in electrical engineering from George Mason Univ., Fairfax, VA. In 2005, he joined IBM, Semiconductor Research and Development Center, Essex Junction, VT working in the technology enablement group. He was assigned as a staff engineer focusing on the development of design groundrules for internal and external latchup prevention and the design of electrostatic discharge protection devices in 65nm and 45nm technologies. Since 2007, he has been with Nvidia Corp., VLSI Design Engineering Center, Santa Clara, CA working in the I/O and Single Integrity team. His work focuses on the design and optimization of ESD circuits and ESD/Latchup protection strategies in I/O's and core logic. Dimitris has been serving to the ESD/Latchup committee of the IRPS Conference (2007).

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Hideaki Kurata received the B.S. (1993) and M.S. (1995) in electronic engineering from Kyoto Univ., Kyoto, Japan. He joined the Central Research Lab, Hitachi, Ltd., Tokyo, Japan, in 1995, he has been engaged in the research and development of high-capacity flash memories. He is a member of the IEEE Electron Device Society and the Institute of Electronics, Information and Communication Engineers of Japan.

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Kae-Dal Kwack (Senior Member, IEEE) Received the B.S. (1974) and M.S. (1976) in electronic engineering from the Hanyang Univ., Seoul, Korea, and the Ph.D. (1980) in electronic engineering from Institute National Polytechnique, Toulous, France. For years, he has served on IEEE ED Hanyang Univ. student chapter chair and IEEE Seoul section officer (Education Activity and currently as a Secretary). As a Secretary in IEEE Seoul section, he was in charge of organizing the successful International Symposium in honor of the 25th Anniversary of IEEE KOREA in June 2000, by the title of 'prospective of electronic industries in North-East Asia' and outstanding contribution to the planning, presiding and success of the IEEE TAB Colloquia visit ceremony, the Seoul in Sep. 1999. Now he is a member of IEEE Asian Pacific Region 10, serving on ECC (Electronic Communication Coordination) chair, MDO (Membership Development Officer) and he has been a chief of RARC (Reliability Analysis Research Center) in Hanyang Univ. since 2005. His current interests are device modeling, analog circuit design, reliability analysis.

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Seongsoo Kweon earned a B.S. (1990) and a M.S. (1992) in materials engineering from Hanyang Univ. in Seoul, Korea. He is now pursuing a Ph.D in materials science and engineering in the UT at Austin since 2002. He worked at Hynix semiconductor (1992-2002). He had involved in Ti-salicide, W-silicide gate process development. He had worked on Oxide and STI CMP process and CMP simulation before he had involved in Cu/Low-K module integration. He is now building a Scanning Hall Probe Microscope (SHPM) for his Ph.D. He will study magnetic materials and DMS (dilute magnetic semiconductor) materials with the home-made SHPM. Before this project, he worked on non-contact nanowire characterization project which was funded by Sematech through Texas AMRC. He is working as an intern in Sematech's FEP division.

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O-Kyun Kwon received the M.S. (1991) and Ph.D. (1999) in material science and engineering from Korea Advanced Institute of Science and Technology, Korea. Since 1991, he has been working at the ETRI in area of high speed optoelectronic devices and vertical-cavity surface-emitting lasers.

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Raymond C. Kwong joined UDC in 2000 as a Senior Scientist, and is currently the Dept. Manager of Material Applications at Universal Display Corp.. He received his B.Sc. (1993) and M.Phil. (1995) in chemistry from the Chinese Univ. of Hong Kong, and Ph.D. in chemistry from the Univ. of Southern CA (2000) under the advisement of Professor Mark E. Thompson. Dr Kwong has over 35 publications and 50 patents and pending patents in the field of organic light emitting devices (OLEDs). At UDC, he leads an R&D team to develop organic electronic materials for high performance OLEDs

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Andrea L. Lacaita received the Laurea degree (summa cum laude) in nuclear engineering from the Politecnico di Milano, Italy, in 1985. In 1989-90, he was Visiting Scientist at the AT&T Bell Labs, Murray Hill, NJ, working on photo-refractive effects in superlattices for optical switching. In 1992, he became Associate Professor of Electronics at the Politecnico of Milano and since then, he has been teaching courses on electronics, electron devices, optoelectronics and solid-state physics. In 1999, he has been Academic Visitor at IBM T.J. Watson Research Center, Yorktown Heights, NY, where he contributed to the development of optical systems for IC testing. In 2000, he was appointed Full Professor of Electronics at the Politecnico di Milano and Head of the Microelectronics Lab. As researcher, he contributed to analog IC design with studies of phase noise in integrated LC-tuned oscillators and with the development of novel architectures of frequency synthesizers in RF front-ends. He has contributed to advances in microelectronics and optoelectronics, with particular emphasis on physics of single photon avalanche detectors, characterization and modeling of semiconductor devices. Within the field of ULSI microelectronics, he has studied carrier transport and quantum effect in scaled MOS transistors, technology and reliability of non-volatile memories. He is co-author of about 150 papers published in journals or presented in international conferences. He is also author of two books in Electronics. Prof. Lacaita received in 1993 the Award of the Italian Association of Electrical and Electronic Engineers (AEI) for his research on hot carrier effects. In 1998-2000, he served as Coordinator of the Committee on micro- and nano-electron devices of the Italian National Group of Electronics Engineers. Since 2000, he has been consultant for the European Commission in the evaluation on review of research projects in micro- and nano-electronics and he has been serving in the program committee of several international conferences.

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Larcher, Luca [MY03]
Luca Larcher graduated in electronic engineering from the Univ. of Padova, Italy (1998), working on the modeling of gate oxide currents in MOS devices. He received his Ph.D. (2001) from the Univ. of Modena and Reggio Emilia, working on the compact modeling of non-volatile memories (E2PROM and Flash). He is currently Assistant Professor of Electronics at the Univ. of Modena and Reggio Emilia, Italy. His research interests concern mainly the electrical characterization, the compact modeling and the failure mechanism analysis of electronic devices and integrated circuit. In this field, he focused on the reliability and the compact modeling of MOS transistors and Floating Gate memories. He has been involved in research projects which resulted in the development of a new Spice-like compact model of Floating-Gate memory devices, used today by STM (partner of the projects). He investigated ionizing radiation effects on Flash memory devices, and he is now involved in projects on alternative Non-Volatile memory technologies, namely NROM and nanocrystal memories. Now, he is working also on the characterization and design of Radio Frequency integrated circuits in CMOS technology. He authored and coauthored a book (Floating Gate Devices: Operation and Compact Modeling, P. Pavan, L. Larcher, and A. Marmiroli, Kluwer Academic Press, Boston, ISBN 1-4020-7731-9, January 2004), and more than 45 technical papers.

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Huy A. Le has been working for a number of companies in semiconductor and telecommunication industries. He has had over 13 technical papers on the topics of electromigration and time-dependent-dielectric breakdown. He graduated with a B.S.E.E. (1990) with highest honors and a doctorate in the same field (2000) from the UT at Arlington, Arlington, TX. Currently, he is with Micron Technology in Boise, ID, working on gate oxide and inter-level dielectric reliability.

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Lee, Choong-Ho [TR01]
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Karen Maex got her Master's in electrical engineering (1982) and the Ph.D. (1987), both from the K.U.Leuven in Belgium. From 1982 until 1987 she was a Research Assistant of the Belgian National Fund for Scientific Research. She continued her research at the Interuniversity Microelectronics Center (IMEC) as a Research Director of the Fund for Scientific Research Flanders. She has been a Professor at the Katholieke Universiteit Leuven since 1989. She was the coordinator and program director of the Erasmus Mundus Master of Nanoscience and Nanotechnology at K.U.Leuven until July 2005. At IMEC she was the director of the Interconnect Technology and Silicide Dept. until December 2000. She co-ordinated the Strategic Research within the Silicon Process and Device Technology Division until July 2005. She was appointed an IMEC Fellow in 2001. She has authored and co-authored more than 200 publications. From August 2005, she has been appointed as Vice-rector Exact Sciences at the K.U.Leuven.

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Zane Marek is a graduate of Texas State Technical College with a degree in electronic engineering technology, and a graduate of the Univ. of Phoenix with a degree in business and marketing. He has extensive knowledge of JEOL tools for bare and patterned wafer review SEMs, edge inspection and defect classification, thin cross-sections and so on.

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Josephine Masicat is currently a Program Manager at Intel's Materials organization and has held various positions in New Technology/Product Integration, Materials Engineering and Quality Control in her 9-year stint at Intel. She received her B.S. in chemical engineering at the Mapua Institute of Technology in Manila, Philippines.

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David G. Mavis is co-founder and Chief Scientist of Micro-RDC. He has over 20 years of experience in the research, development, and design of nuclear and space radiation hardened microelectronics. He received his bachelor's degree in physics from the Univ. of Wisconsin, Madison, and his doctorate in nuclear physics from Stanford Univ.. His major interests are currently in the area of Single Event Effects in ultra-deep submicron microcircuits.

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Joe McPherson received the Ph.D. (1975) in physics from Florida State Univ.. Prior to joining Texas Instruments, he was an assistant professor with the Univ. of NC and a visiting scientist with the Argonne National Lab. He joined TI in 1980, in the area of process development and was instrumental in bringing silicides and laser redundancy into VLSI production. Since 1983, his primary focus has been in reliability physics where he has published over 200 papers and holds 10 patents in the areas: time-dependent dielectric breakdown, electromigration, stress migration, fatigue, corrosion, surface inversion, channel hot carriers, data retention, heat dissipation, soft-errors, Cu and Low-k, high-k gate dielectrics and ferroelectrics. He was the 1995 General Chairman of the IEEE IRPS and the 1998 & 2006 Chairman of the Reliability Technology Advisory Board (RTAB) reporting to Sematech. In 2004, Joe received the IEEE Engineer of the Year Award from the Texas Society of Professional Engineers. Joe is currently a Senior Fellow at TI and the Reliability Manager for Advanced Materials. He is also currently on the Board of Directors of the IRPS.

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Gaudenzio Meneghesso graduated in electronics engineering at the Univ. of Padova in 1992 working on the failure mechanism induced by hot-electrons in MESFETs and HEMTs. He received the Italian Telecom award for his thesis work in 1993. In 1995 he was at the Univ. of Twente (The Netherland) with an Human Capital and Mobility fellowship (within the SUSTAIN Network) working on the dynamic behavior of protection structures against ESD. In 1997 he received the Ph.D. in electrical and telecommunication engineering from the Univ. of Padova working on hot-electron characterization, effects and reliability of GaAs-based and InP-based HEMT's and pseudomorphic HEMT's. Since 2002 is with Univ. of Padova as Associate Professor. His research interest are: a) Electrical characterization and modeling of microwave devices on III-V semiconductors such as GaAs and InP (MESFETs, HEMTs and PHEMTs); b) Reliability studies of the long term stability of microwave devices; c) Electrical characterization, modeling and reliability of electronic and opto-electronic devices grown on wide bandgap semiconductors (SiC and GaN); d) Design, characterization and modeling of Electrostatic Discharge (ESD) protection structures for CMOS and SMART POWER (BCD technology, Bipolar, CMOS and DMOS) integrated circuits; Within these activities he published over 180 technical papers (18 Invited Papers and 2 best paper awards at 1996 and 1999 ESREF Conference). He has been the Technical program Chair of WOCSDICE 2001, General Chair of HETECH 2001. He is in the Technical Program Committees of: EuMW 05 and 06, IEEE- IRPS 2005 and 2006, EOS-ESD Symp 2006. He served several years for IEEE IEDM: in 2004 and 2005 he was the Chair of the Quantum Electronics and Compound Semiconductors sub-committee, in 2006 he is the European Arrangements Chair.

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Matteo Meneghini graduated in electronics engineering at the Univ. of Padova, Italy in 2004 with a thesis on the electrical and optical characterization of gallium nitride LEDs. In 2004 he obtained the Italian Engineering Qualification and cooperated with the Dept. of Information Engineering of the Univ. of Padova, working on performance evaluation of high brightness LEDs. In 2005 he enrolled in a Ph.D. course on information engineering at the Univ. of Padova. He is currently involved in the Italian Research Ministry Project on Reliability and operating conditions of GaN-based Light Emitting Diodes (LEDs) for solid-state lighting, and he is working, in cooperation with OSRAM-OS, on electro-optical characterization, modelling and reliability of GaN LEDs. Furthermore, he is studying the behaviour of high-power LEDs under electrical stress, and the best operating conditions for these devices.

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Jan Mertens received the degree of industrial engineer (1991) in electronics with a major in telecommunication from Groep T Leuven, Belgium. He joined the Belgian army for one year and got the degree of lieutenant. Between 1993 and 1997, he worked first as a teacher in electronics and later on as a service engineer in a company specialized in process safety and facilities protection using active explosion protection systems. In 1997 he joined the physics lab of the Universiteit Hasselt (former Limburgs Universitair Centrum) Belgium where he was engaged in the development of physics labo setups. In 2001 he started working at the section Electrical Characterisation and Reliability of IMOMEC, a division of the Interuniversity Micro-Electronics Center (IMEC), Belgium. He is engaged in research and development of in-situ high resolution measurement techniques for electrical characterisation and reliability of electronic materials. IMOMEC is highly specialised in this field and is participating in a number of national and European research programs.

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Miroslav Micovic received B.Sc. (1989) in physics from The Univ. of Ljubljana, Slovenia and Ph.D. (1997) in electrical engineering from The Pennsylvania State Univ.. Since he joined HRL Labs in 1998, he has worked on the development of advanced compound semiconductor devices. Dr. Micovic is currently the technical leader of GaN efforts at HRL Labs. He has authored or co-authored more than 50 technical and scientific papers and holds several U.S and international patents.

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Enrique Miranda received the Ph.D. (1999) in electronics engineering from the Universitat Autònoma de Barcelona (UAB), Spain and the Ph.D. (2002) in physics from the Universidad de Buenos Aires (UBA), Argentina. He was Associate Professor at the Faculty of Engineering UBA and member of the National Council of Science and Technology (CONICET), Argentina. Now he is Professor at the Departament d'Enginyeria Electrònica UAB. He was awarded several fellowships: Intercampus and Mutis from Spanish International Cooperation Agency, post-doctoral from Università degli Studi di Padova, visiting Professor at the Technical Univ. Hamburg-Harburg from the German Academic Exchange Service (DAAD), researcher at the Tokyo Institute of Technology (Matsumae Foundation), and Tan Chin Tuan from the Nanyang Technological Univ., Singapore. Dr. Miranda is also member of the Editorial Board of Microelectronics Reliability, member of the INFO's scientific committee and participates in the EDS-IEEE Distinguished Lecturer program. His research interests are conduction mechanisms in dielectrics and reliability of MOS devices.

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Jerome Mitard graduated from the Polytechnic Univ. School in Marseilles, France, (2003) with a major in microelectronic and communication engineering. Currently he is acting as a ST assignee at CEA-LETI in Grenoble, where he is involved in the electrical characterization of alternative gate dielectrics for sub-45nm CMOS technologies. In addition, he is conducting his research toward his Ph.D. (last year) in electrical engineering where he is focusing on the charge trapping of high-K / metal gate dielectrics.

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Subhasish Mitra is an Assistant Professor in the Dept.s of Electrical Engineering and Computer Science of Stanford Univ.. His research interests include robust system design, VLSI design and test, VLSI CAD, computer architecture and robust design for emerging nanotechnologies. Prior to joining Stanford, he was a Principal Engineer at Intel Corp. where he developed enabling technologies for robust system design that have been deployed in actual products. He received Ph.D. in electrical engineering from Stanford Univ.. Prof. Mitra has published more than 80 technical papers in leading conferences and journals, and invented design and test techniques that have seen wide-spread proliferation in the industry. His X-Compact technique for test compression has been used by more than 40 Intel products including microprocessors, chipsets, and communications chips, and is supported by major CAD tools. Prof. Mitra's recent honors include the IEEE Circuits and Systems Society Donald O. Pederson Award for the best paper published in the IEEE Transactions on Computer-Aided Design, a Best Paper Award nomination at the Design Automation Conference, a Divisional Recognition Award from the Intel "for a Breakthrough Soft Error Protection Technology," a Best Paper Award at the Intel Design and Test Technology Conference for his work on Built-In Soft Error Resilience, the Sundaram Seshu Scholar Lecturer at the Coordinated Science Lab of the Univ. of Illinois at Urbana Champaign, Terman Fellow at Stanford, and the Intel Achievement Award, Intel's highest honor, "for the development and deployment of a breakthrough test compression technology that achieved an order of magnitude reduction in scan test cost." Prof. Mitra has held several consulting positions, and served on the organizing and program committees of several IEEE and ACM sponsored conferences. He co-founded the IEEE SELSE (System Effects of Logic Soft Errors) Workshop which expanded its scope in 2007 to include a broad class of Silicon Errors in Logic and System Effects. This workshop enabled standardization of public logic soft error rate numbers for the research community for open exchange of quantifiable research results from both industry and academia.

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Takayuki Mizuno received B.S. (1999) and M.S.(2001) in chemistry from Yamanashi Univ., Yamanashi, Japan. Since 2001, he has been engaged in development of Nano-Prober (measurement of electronic characteristics in individual devices) and it's applications for failure analysis of integrated circuits.

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Peter Moens received a M.Sc. (1990) and a Ph.D. (1993) in solid state physics from the Univ. of Gent, Belgium. From 1993 till 1996, he worked as a post-doctoral fellow in collaboration with Agfa-Gevaert, Mortsel Belgium on the

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Karl C. Mohr is presently a Ph.D. candidate in electrical engineering at Arizona State Univ.. His research interests include high-speed low-power VLSI circuits, systems, CAD and radiation hardening. He received his BSEE from ASU in 1999, and has 13 years experience in the IC industry.

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Hiroki Morimura received the B.E. (1991) in physical electronics, the M.E. (1993) in applied electronics and the Dr. Eng. (2004) in advanced applied electronics from the Tokyo Institute of Technology, Japan. In 1993, he joined Nippon Telegraph and Telephone Corp. (NTT), Tokyo, Japan. He has been engaged in the research and development of low-voltage, low-power SRAM circuits. He is now a Senior Research Engineer at NTT Microsystem Integration Labs, Kanagawa, Japan. He is currently doing research on sensing circuits for CMOS fingerprint sensors and developing single-chip fingerprint sensor/identifier LSIs for portable equipment. Dr. Morimura is a member of the IEEE, the Institute of Electronics, Information and Communication Engineers of Japan, and the Japanese Society of Applied Physics.

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Mujahid Muhammad is a Device Design Engineer at the Semiconductor R&D Center at IBM's Microelectronics facility at Essex Junction, VT. He received the B.E. (1994) in electrical and electronics engineering from B.V.B. College of Engineering and Technology, Hubli, India and the M.S. (1999) in electrical and computer engineering from Univ. of Houston, TX. Since then he has been working as a member of the ESD and Latchup Development team and has been involved in the development, design, characterization and implementation of test structures for the study of ESD and Latchup phenomenon in advanced CMOS technologies. Presently, he is focused on documenting ESD design groundrules and guidelines and conducting ESD protection design reviews on various customer chip designs. He has authored or co-authored twenty technical papers and posters. He also has four patent applications and three issued patents on ESD and Latchup issues.

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Tsutomu Murakawa has received the M.S. (2005) in nanomechanics from the Tohoku Univ. graduate school. He joined the Semiconductor Energy Lab in 2005.

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Suhail Murtaza received the B.S. (1998) in electrical engineering from the Aligarh Muslim Univ., India. After working at the same university for one year as a lecturer, he moved to the UT in Austin, TX where he received his M.S. (1991) in manufacturing engineering. He received the Ph.D. (1995) in electrical and computer engineering from the same Univ.. From 1996 to 2000 he was an advanced CMOS process integration engineer and a mixed-mode analog product engineer at Texas Instruments, TX. From 2000 to 2002 he developed flash memory processes at Atmel. From 2002 to 2005 he worked on SPICE modeling at TI. Since 2005 his interest has been focusing on ESD development for TI mixed-mode analog technologies. He has authored and co-authored more than 20 papers on the physical properties of Silicon-Germanium alloys and on advanced CMOS process integration and holds several patents.

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Toshihide Nabatame received the B.S. (1985) and M.S. (1987) in chemistry from Tohoku Univ., Miyagi, Japan, and the Ph.D. (1994) from Tokyo Institute of Technology, Tokyo, Japan. In 1987, he joined the Hitachi Research Lab, Hitachi Ltd., Ibaraki, where he has been engaged in research and development on deposition techniques and characterization of High-Tc superconductor, FeRAM and DRAM devices. In 2001, he joined the High-k Gate Stack Gr. of MIRAI project as a group sub-leader, where he has been investigating on gate stack technology with high-k materials. Since 2003, he has been with the Process Development Dept., Renesas Technology Corp., Tokyo, Japan. From 2003 to 2004, he was a Guest Professor with the R&D Center, Kagoshima Univ., Kagoshima, Japan. Dr. Nabatame is a member of the Japan Society of Applied Physics and the Institute of Electrical Engineers of Japan.

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Makoto Nagamine received the B.S. (1989), M.S. (1991), and the Ph.D. (1994) in chemistry from Faculty of Science, Univ. of Tokyo, Japan. In 1994, he joined Toshiba Corp as a process engineer in the ULSI Research Labs. He worked on radical oxidation process for highly-reliable CMOS gate oxide. Since 2002, he has worked on MRAM. He is developing tunnel barrier with high magnetoresisitive ratio and high reliability at Advanced LSI Technology Lab in Corporate Research & Development Center.

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Koji Nakamae received the B.E. (1977), M.E. (1979), and the Ph.D. (1982) in electronic engineering from Osaka Univ., Osaka, Japan. In 1982, he joined the Electron Beam Lab, Faculty of Engineering, Osaka Univ.. From 1991 to 1992, he was an Assistant Professor at the Dept. of Information Systems Engineering, Faculty of Engineering, Osaka Univ.. From 1992 to 2005, he was an Associate Professor there. Since 2006, he has been a Professor at the Graduate School of Information Science and Technology. He has been engaged in researching methods, systems, and applications of electron beam testing of integrated circuits. His work also includes image processing and analyzing the economics of VLSI towards high efficient and low cost manufacturing test system.

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Mamoru Nakanishi received the B.E. (1986), M.E. (1988) in physical electronics from Tokyo Institute of Technology, Tokyo, Japan. In 1988, he joined NTT LSI Labs, Kanagawa, Japan. He is engaged in the research of a highly parallel architectures and their applications, especially for image processing. He is now senior research engineer, supervisor, in NTT Microsystem Integration Labs, Atsugi, Kanagawa, Japan. Mr. Nakanishi is a member of and the IEEE Computer Society, the Institute of Electronics, Information and Communiation Engineers of Japan, and Information Processing Society of Japan.

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Masashi Nakata received the B.S. (2001), and the M.S. (2003) of engineering from Tokyo Institute of Technology, Japan. Since 2003 he has been working for the 2nd Micro Computer Division, NEC Electronics Ltd. He is now responsible for the development of non volatile memory devices.

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Deepak K. Nayak earned the B.S. (1983) from the Indian Institute of Technology, Kharagpur, India, the M.S. (1985) from the Drexel Univ., Philadelphia, and the Ph.D. (1992) from the UCLA, all in electrical engineering. He is currently pursuing his MBA at the Haas School of Business, UC-Berkeley. Deepak has over 15 years of industry experience in the field of CMOS logic R&D and manufacturing. He has worked at the Microelectronics Center of NC, U. of Tokyo, AMD, Altera, and Xilinx. At the Univ. of Tokyo, he occupied the Hitachi Ltd. Endowed Faculty Chair in Quantum Materials, focusing his

research work on Strain-Si technology. He joined AMD's Logic Development Group as a Member of Technical Staff, in 1994, and led the transistor development work for the AMD's K6 processor. He joined Xilinx, in 1999, as a Senior Manager in the Technology Development Dept. and was promoted to a Principal Engineer in 2005. He has been leading a Foundry Group to develop advanced CMOS technology for Xilinx FPGAs. He is also the head of the Technology Reliability group at Xilinx. Deepak has made many fundamental contributions to the research and development of Strained-Si and SiGe technology. He was the first to propose and experimentally demonstrate the high-mobility strained-Si PMOSFET on Si substrate. Other contributions include, for the first time, the strained-SiGe PMOSFET on Si and SOI. He has published over 75 papers in the area of Strained-Si, SiGe, and CMOS technology, and holds/applied over 20 patents. He serves as a member of the Technical Advisor Board of AmberWave, a startup company commercializing the production of substrates for Strained-Si CMOS. His current interest is in CMOS

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Takenao Nemoto has received the M.S. (1989) and the Ph.D. (2007) in nanomechanics from the Tohoku Univ. graduate school. He joined to the Kawasaki Steel Corp. in 1989, where he worked for physics of LSI interconnection reliability. He moved to the Tokyo Electron Ltd. in 1995, where he worked for metal CVD development. He entered to Tohoku Univ. in 2004 to study the physics of electromigration. He is a member of the Japan Society Applied Physics, the Japan Society of Metal and the Japan Society for Strength and Fracture of Material.

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David Ney is a graduate of the engineering school of physics of Grenoble, France (ENSPG) in 2003. He received the M.S. in micro and nanoelectronics (2004) from the Univ. Joseph Fourier of Grenoble. Since 2003, he is a Ph.D. student in the reliability group of the Central R&D of STM, Crolles, France. He is working on electromigration issues in advanced copper interconnects in collaboration with TECSEN Lab in Marseille, France.

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Chee Mang Ng received his B.Sc. (Hon.)(1992) and M.Sc. (1996) in physics from Univ. of Malaya, and Ph.D. (2001) in physics from National Univ. of Singapore (NUS). Since then, he joined Chartered as process engineer and later as process integration engineer under fab operation and he was involved in developing device technology of various technology generations for communication applications. He is now the program manager of Chartered's university research program with the universities in Singapore. He holds adjunct assistant professorship at the School of Electrical and Electronic Engineering of Nanyang Technological Univ., Singapore (NTU) and Physics Dept. of NUS. His research interests include structural and electronic studies of strained silicon, advanced materials for next-generation interconnect and fabrication of silicon based nanowire transistors.

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Paul E. Nicollian received the B.S. in physics from Penn State Univ. (1983) and the M.S. in physics from the UT, Dallas (1990). He was employed by United Technologies Mostek Corp. in 1984. He joined Texas Instruments in 1985, where he is currently a Senior Member of the Technical Staff in Silicon Technology Development. His current research is focused on the reliability physics of ultrathin gate dielectrics. He has co-authored 28 publications, holds 2 US patents, and is a recipient of the 2000 IRPS Best Paper Award. He served on the IRPS Technical Program Committee from 2000 - 2005, co-chairing the Device Dielectrics Committee in 2001 and the Process Induced Damage Committee in 2000. He also served on the 2004 - 2005 IEDM CMOS and Interconnect Reliability Committee. Mr. Nicollian is a Senior Member of the IEEE.

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Akihiro Nitayama received the B.E. (1978) in electrical engineering, the M.E. (1980) and the Ph.D. (1983) in electronics engineering from Tokyo Univ., Tokyo, Japan. In 1983 he joined Toshiba Corp. as a device engineer in the R&D Center and had worked on DRAM till 2001. Since 2003, He has been engaged in MRAM. He is currently a senior manager of the advanced memory device technology department in the Center for Semiconductor R&D (CSRD), in charge of process integration and device design on FeRAM, MRAM, advanced flash, and other novel memory devices.

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Takeshi Nokuo is a graduate of Osaka Univ. with a degree in applied physics. He began his career at JEOL in 1990, as a research and development engineer, mainly engaging in the development fields of scanning electron microscopes and their applications.

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Mitzi Nuda has been a Package Reliability Engineer under Intel's Flash Memory Group in Cavite, Philippines since April 2003. She obtained her Bachelor's (2000) in metallurgical engineering from the Univ. of the Philippines and is currently taking up her Masters in material science and engineering.

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Ennis T. Ogawa is currently working in the Advanced Materials Reliability R&D Group under Silicon Technology Development (SiTD) at Texas Instruments (TI), Inc. in Dallas, TX. He received his B.S. (1986) in physics from Stanford Univ. and his Ph.D. (1994) in physics at The UT at Austin in the field of high-temperature superconductivity. Following his doctoral degree, he worked as a postdoctoral fellow in the Interconnect and Packaging Lab, directed by Prof. Paul S. Ho, at The UT at Austin and continued as a Research Associate until mid-2001. His research interests there focused on the thermal conduction of low-k polymers, metal-polymer adhesion, low-k materials characterization, interconnect thermal stress, and Al(Cu)-based and Cu-based electromigration. His current interests at TI address issues pertaining to the reliability of Cu/low-k backend Si technology such as electromigration, stress-induced voiding, intermetal and interlevel dielectric reliability, and thermal management. He remains very fascinated with fatherhood.

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Federica Ottogalli received the Laurea degree (1998) in physics from the Univ. of Padova, Italy,with a thesis on crystallographic characterization by RBS-channeling and modeling of III-V compounds (GaN-based) epitaxially grown on Al O. She joined the Non-Volatile Memory Technology Development Group of the Central R&D of STM, Agrate Brianza (Milan), Italy, in 1999. She worked on the process integration of Flash memories (for the 0.18-μm and 0.16-μm node technology) and of phase-change nonvolatile memory cells based on chalcogenide materials. Her current activity, since 2002, is focused mainly on electrical characterization of PCM memory cells.

Paccagnella, Alessandro [MY05]
Alessandro Paccagnella received the Laurea degree in physics cum Laude (1983) from the Univ. of Padova. He is now Full Professor of Electronics at the Univ. of Padova. He is co-author of more than 300 scientific papers. In the past, his research activity has been directed to the study of different aspects of physics, technology, and reliability of semiconductor devices. In relation with this activity he spent some research periods at the Univ. of CA, San Diego, and at the IBM T.J. Watson Research Center, Yorktown Heights, NY. At present, he coordinates the research activity of a group at the Dept. of Information Engineering, Univ. of Padova, working on CMOS devices and technology. His research work is focused on the study of ultra-thin gate dielectrics in MOS submicron devices, on the damage induced by ionizing radiation and the corresponding measurement methods and techniques on components, with emphasis on non-volatile memories and programmable logic devices.

Padovani, Andrea [MY03]
Andrea Padovani graduated in electronic engineering at the Univ. of Modena and Reggio Emilia, Modena, Italy, in 2005 working on reliability of NROM non-volatile memory devices. In 2006, he started his Ph.D. at the Univ. of Ferrara, Ferrara, Italy. His research interests concern both conventional (Floating Gate) and innovative non-volatile memory technologies such as NROM, Phase-Change Memories and other resistive-switching devices.

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Luigi Pantisano received the Laurea degree (in cooperation with the Reliability Lab, ETH, Zurich, Switzerland) and in 2000 a Ph.D. in electrical engineering from Univ. of Padova, Italy. In 2000, he was with Bell Labs-Lucent Technologies, Murray Hill, NJ, pursuing the impact of plasma-charging damage on RF CMOS devices. Since 2001, he has been with the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, working on high-k gate dielectrics for CMOS technologies. He contributed to more than 90 papers in the field of plasma damage, RF measurements, reliability and electrical characterization of novel high-k devices.

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Byung-Gook Park received the B.S. (1982), the M.S. (1984) in electronics engineering from Seoul National Univ., Seoul, Korea, and the Ph.D. (1990) in electrical engineering from Stanford Univ., Stanford, CA. He is currently a full professor. He has been in charge of the research of Inter-university Semiconductor Research Center (ISRC) in Seoul National Univ. since 2003 as the chief of the research department. His current research interests are nanoscale CMOS devices, Si single-electron devices, nonvolatile memory devices, and organic electroluminescent displays.

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Donggun Park received the B.S., M.S., from Sogang Univ., Seoul, Korea, and Ph.D. from the UC, Berkeley all in electrical engineering. His Ph.D. study was for the plasma charging damage and reliability of thin gate oxides. Since he joined Samsung Electronics in 1983, he was involved in the diffusion process development of 64K and 256K DRAM, and process integration of 1Mega, 4Mega, 16Mega DRAM developments until 1993. After he finished his Ph.D study in 1998, he rejoined Samsung Electronics to develop 0.15μm and 0.13μm 256M DRAMs, 90nm NAND Flash, and 100nm high speed 72M SRAM, in 1999, 2001, 2002, 2003, respectively. Now he is leading a development team for next generation sub 50nm DRAMs and nano-CMOS transistors such as FinFET/MBCFET/nanowireMOSFET/SOONO Transistors.

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Jong-Man Park received the B.S. from Chungang Univ., M.S. from Sungkyunkwan Univ., Seoul, Korea all in electrical engineering. Since he joined Samsung Electronics in 2000, he involved in the failure analysis of DRAM products. After he finished his M.S. study in 2005, he joined to develop 68nm DRAM process integration. Since 2006, he has been with Device Research Team for the next generation sub 50nm DRAMs. His research interests include advanced CMOS structure and technology for future memory devices.

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Sung-Ki Park received the B.S. (1983) in materials engineering from Yonsei Univ., Seoul, Korea. In 1985, he joined Hynix Semiconductor Inc., where he worked on the thin film process engineer for DRAM devices. Since 1999, he has been engaged in research and development of advanced planarization module, CMP, wafer cleaning and metallization technology for DRAM, SRAM and Flash Device. From 2002, he is in charge of the Flash process group at the Memory R&D division. His research interests include development of advanced processes for Flash memory devices, in particularly lithography and process reliability analysis for 60nm technology and beyond.

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Ron has a very diverse background working on everything from GaAs optoelectronics, acoustic-optics, silicon-on-sapphire (and other SOI) radiation hardened technologies, Si-based micro control-lers, and NVM. He has served as a process integration, device, product, and reliability engineer. Ron started his career with the Naval Research Lab on Co-Op assignments from the Univ. of Iowa before attending graduate school at Lehigh Univ.. Upon completion of his Ph.D. in 1995, he joined Motorola in Phoenix bringing up a 0.8 μm embedded NVM technology. Ron joined Impinj in December 2003.

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Paolo Pavan received the degree in electrical engineering from the Univ. of Padova, Padova, Italy, (1990), and the Ph.D. (1994) from the same university. His Ph.D. work concerned impact ionization phenomena in advanced bipolar transistor. From 1992 to 1994, he was with the UC, Berkeley, where he studied radiation effects on MOS devices and circuits. More recently, his interest has been in the characterization and modelling of Flash memory cells and on the development of new nonvolatile cells, also in cooperation with international companies (Saifun Semiconductors, Israel). He has authored and co-authored technical papers, invited papers, one book and two chapters in books. He is currently Professor of Electronics at the Università di Modena e Reggio Emilia, Reggio Emilia, a member of IU.NET (Italian Univ. Nano Electronics Team) Consortium. He served as a reviewer of many Journals and Conferences, and as a member of technical and executive committees of many Meetings, most recently in IEDM.

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Vincent Pouget received his Master's in applied physics (1997) and his Ph.D. in instrumentation and measurement (2000) from the Univ. of Bordeaux 1, France. He's now a Researcher with the CNRS at the IMS (formerly IXL) Lab of the Univ. of Bordeaux, where he's responsible of the ATLAS laser facility. His main research interests are: pulsed laser applications for nanoelectronics, integrated circuits testing and failure analysis and instrumentation software development.

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Marco Racanelli received his Ph.D. and M.S. in electrical and computer engineering from Carnegie Mellon Univ., and his B.S. in electrical engineering from Lehigh Univ.. He is currently Vice President of Technology and Engineering at Jazz Semiconductor where he leads technology development, modeling, design automation and design service teams. Dr. Racanelli has worked in the area of technology development through his carreer that started at Motorola then Rockwell which spun off Conexant Systems and eventually Jazz Semiconductor. Dr. Racanelli has authored more than 50 technical publications and holds 30 US Patents.

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Mustapha Rafik received the engineer degree in physics from the Institut Nationale Polytechnique de Grenoble (INPG) and the M.S.E.E in micro and nanoelectronics from Joseph Fourier Univ. (Grenoble, France) in 2005. He is now a Ph.D. student in the reliability group of the central R&D of STM, Crolles, France. His research interests include reliability of advanced gate stacks.

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Vijay Reddy is a Senior Member of the Technical Staff at Texas Instruments, Dallas, TX. After receiving the Ph.D. (1994) in electrical engineering from UT Austin, he joined TI and has worked on several reliability topics spanning from transistor to circuit to product reliability. He has presented invited tutorials on CMOS Reliability at IRPS (2002-04) and ICMTS (2006). He has served on the IRPS program committee member for several years and is currently serving on the IEDM CMOS and Interconnect Reliability sub-committee (2006-07). He received the 2002 IRPS Outstanding Paper Award for his work on the circuit impact of NBTI and was a co-recipient of the 2004 IRPS Outstanding Paper Award and the 2002 ESD/EOS Symposium Best Paper/Best Presentation Awards. He has received four patents with several pending along with more than 20 publications including at such conferences as IRPS and IEDM.

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Gilles Reimbold received a Ph.D. (1983) from the National Polytechnic Institute of Grenoble, on the topic of noise in MOS transistors and CCD. He joined the EA-LETI to work on CMOS VLSI technologies development on the topic of transistors optimization. He was then in charge of an internal company project to develop all reliability test and modeling activities for CMOS Front End and Back End. He then managed the electrical lab covering statistical test, electrical test and CMOS reliability aspects. He his now head of advanced electrical characterization and modeling group covering high k materials, SOI devices and non volatile memories. He has been co-author of more than 100 papers in these fields and is or has been a member of scientific and organization committees of several international conferences as P2ID, INFOS, and IRPS. He was also involved in reliability teaching, was Summer School Scientific Chair (MIGAS 1999), and chairman in many conference sessions.

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Hans Reisinger received his diploma in physics (1979) and his Ph.D. (1983) both from the Technical Univ. of Munich. In 1986 he joined the Siemens Semiconductor Dept. (now Infineon). His work was focused mostly on the study of thin dielectrics and interfaces in DRAMs and NVMs. Currently he is with the Reliability Methodology group and works on MOSFET degradation.

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Guillaume Ribes received the engineer degree in electrical engineering from the ISEN de Toulon (Institut Supérieur d'Electronique et du Numérique,

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Yonghan Roh received the B.S. in electronic engineering from Sungkyunkwan Univ., Seoul, Korea, and M.S. and Ph.D. in electrical and computer engineering, Univ. of Houston. His Ph.D. study was for the degradation mechanisms of SiO_2 in MOS devices. Since he joined Sungkyunkwan Univ. as a professor, he has been researching MOS devices and physics, nano- and bio-electronics, and monolithic microwave integrated circuits (MMIC).

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Michael Röhner received the diploma in physics from the Univ. of Erlangen-Nürnberg (1994) and the Ph.D. from the Univ. of Würzburg (1999). His Ph.D. thesis was on vertical cavity surface emitting lasers. In 1998 he joined Infineon Technologies working on CMOS technology integration and device reliability. His current activities focus on the reliability of ultra-thin oxide layers.

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Russo, Ugo [6B.2]
Ugo Russo received the second (master) level Laurea degree in electrical engineering from the Politecnico di Milano, Italy, cum laude, in 2005. During the thesis of Laurea he worked on Phase Change Memories (PCMs) in the Dept. of Electrical Engineering, Politecnico di Milano, Italy, where he is currently pursuing the Ph.D. His research interests include the modeling of electrical and phase-change properties in PCM devices. He cooperates with the Dept. of Mathematics of Politecnico in holding master classes on Numerical methods for microelectronics.

Ryu, Choon-Kun [FA02]
Choon-Kun Ryu received the B.S., the M.S., and the Ph.D. in materials science and engineering from Seoul National Univ., Korea, Stanford Univ., USA, and Univ. of Illinois at Urbana-Champaign, USA, respectively. From 1995 to 1998, he was a process technologist at Applied Materials, Santa Clara, CA. Since 1998, he has been a senior member of technical staff at R&D Division, Hynix Semiconductor Inc., Icheon, Korea.

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Ganesh Samudra is currently an associate professor at National Univ. of Singapore (NUS), Dept. of Electrical and Computer Engineering. He obtained Ph.D. from Purdue Univ., USA in 1985 and worked for 3 years in Texas Instruments before joining NUS. His research is in the area of simulation and novel devices. He has published about 100 technical papers.

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David Trémouilles received the M.S. in electrical engineering (2000) and his Ph.D. in microelectronic circuit and microsystem design (2004), both from the Institut National des Sciences Appliquées (INSA) of Toulouse, France. During his Ph.D. his research activity focuses on the design optimization, simulation and modeling of ESD protections for BiCMOS technologies. This work was carried out at the Laboratoire d'Analyse et d'Architecture des Systèmes of CNRS (LAAS/CNRS) in collaboration with On Semiconductor Toulouse, France. Since October 2004 he is with the reliability researcher group at IMEC (Interuniversity Microelectronics Center), Leuven, Belgium, where he was granted a Marie Curie Intra-European fellowship from the European Community. His research interests are on the impact of new technology options and device architecture on ESD robustness, and innovative ESD protection for RF circuits.

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Heinrich Wolf received his diploma degree in electrical engineering from the Technical Univ. of Munich (TUM) and his Ph.D. from the Technical Univ. of Berlin, Germany. He joined the Chair of Integrated Circuits at the TUM as a member of the scientific staff working on ESD related issues. This involved modeling of ESD-protection elements, parameter extraction techniques and design protection elements. In 1999 he joined the Fraunhofer-Institute for Reliability and Microintegration (IZM) where he was involved in the investigation of ESD phenomena in the CDM time domain for CMOS and Smart Power Technologies. Furthermore he was involved in the field of RF characterization and he worked on the development of ESD test methods and tester characterization. Currently he is coordinating the ESD related activities at the IZM.

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